ARGUMENTS/REMARKS:

Claims 1-10 were rejected under 35 U.S.C. 102(e) as anticipated by Iorga et al., Patent No. 6,642,707. Applicants demonstrate below that their invention was made prior to the September 13, 2000 filing date of Iorga et al., thus eliminating this reference as prior art. Also, in case the subject matter of Iorga et al. is prior art under some other basis presently unknown to applicants, new claims 11-20 are presented herein which patentably distinguish over Iorga et al.

As set forth in the enclosed Declaration of Co-Inventor Robert A. Duris, the concept of the invention was the subject of a slide presentation he made at a confidential internal technical conference for the invention's assignee Analog Devices, Inc. (ADI) on April 13, 2000 (five months before the Iorga et al. filing date). The Duris declaration includes annotated copies of selected figures from the slide presentation, marked-up to show the correspondence between the figure elements and the elements of the principal claims in the present application as originally filed. All of the elements of these claims appear in the figures, and the slide presentation also included a photograph of a chip layout to implement the invention. These documents demonstrate that the invention was conceived not later than April 13, 2000, the date of the slide presentation.

The remainder of the Declaration demonstrates that diligence was exercised from the date of the slide presentation to the fabrication and successful testing of

devices embodying the invention as claimed. The principal milestones in this process, summarized in the Declaration, were:

- May 25, 2000: A circuit designed to implement the invention was released to the ADI (assignee) fabrication facility.

- August 22, 2000: A first wafer lot was received from the ADI fabrication facility with internal T-coils, and tested to demonstrate that both the current- mode and voltage-mode drivers were functional.

- September 15, 2000: A second wafer lot, with internal T- coils but also configured to receive external T-coils, was received. Development of test software for this lot began the same day.

- September 20, 2000: The test software for the second lot was completed and the circuits were DC tested, with a successful yield for 17 out of the 24 circuits with internal T-coils. The second lot wafers were then sent outside of ADI for the addition of external (post-passivation) T-coils.

- October 12, 2000: The completed wafers, including post-passivation T-coils, were returned to ADI. Development of a characterization setup by ADI to test and characterize the circuits began the same day.

- October 17, 2000: Circuits with and without post-passivation T-coils were tested, demonstrating that the post-passivation T-coils were successful in substantially compensating the receiver circuit capacitance.

The Duris Declaration demonstrates that the present invention was conceived before the Iorga et al. application was filed in the United States, and that diligence was exercised in reducing the invention to practice through the fabrication and successful testing of circuits within the scope of the principal claims. Since the present invention

was thus made prior to the filing of Iorga et al., that patent is not a valid reference against claims 1-10 under 35 U.S.C. 102(e).

A non-substantive semantic amendment has been made to claims 2, 6 and 8, changing "passive matching circuit" to "passive matching network". These claims are now consistent with their parent claims 1, 5 and 7, which use the "passive matching network" terminology.

New claims 11-20 have been added to emphasize a patentable distinction over the subject matter of Iorga et al., in case this subject matter turns out to be prior art through some other means, even though the Iorga et al. patent per se is not. Claims 11-20 are the same as claims 1-10 except for the addition of a requirement that the passive matching networks be "bidirectional".

In the Office action, the circuit (L1,C1) of Iorga et al. was considered to comprise a T-coil circuit. However, this is not actually the case. Iorga et al. discloses RC peaking circuits C1,R1 and C2,R2, with matching circuits L1,R3 and L2,R4 added, with respective time constants the same as C1,R1 and C2,R2 to impedance match the C,R circuits to their respective lines 34 and 38. The inductive branch circuitry neutralizes impedance mismatching caused by the capacitive branch circuitry. (column 3, lines 8-15; column 3, line 37-column 4, line 5).

The peaking circuits C1,R1 and C2,R2 are separate from their respective impedance matching circuits L1,R3 and L2,R4, and do not form T-coils with them. As described in

the specification of the present application at page 5, line 26-page 6, line 2, a T-coil circuit consists of a pair of inductors that are coupled to one another by a degree of mutual inductance. There are no such coupled inductors in Iorga et al. Contrary to the implication of the Office action, a capacitor is not necessary to implement a T-coil circuit. As stated in the present specification, the addition of a bridging capacitor to the T-coil circuit is optional, the purpose being to enable circuit operation during an initial inductor charging period, and a bidirectional improvement in bandwidth. (page 5 line 33-page 6, line 9). Thus, the combination of C1,R1 and L1,R3 does not form a T-coil circuit, not does the combination of C2,R2 and L2,R4.

A T-coil circuit is bidirectional, propagating both test signals to the cable connected to the device under test (DUT), and signals returned back from the DUT to the receive circuit (illustrated in applicants' Figs. 1-3 as Comp 1 and Comp 2). The bidirectional nature of the drive channel as the primary application for the present direction is stressed throughout the application, for example at page 3, lines 2-5 and 21-23; page 5, lines 7-8; page 6, lines 2-9. By contrast, Iorga et al. is not bidirectional; it employs separate deliver and receive signal paths. For example, see column 1, lines 37-40; column 2, lines 30-34; column 3, lines 17-21 and 37-40.

The need for separate cables for transmitting a drive signal to the DUT, and directing the DUT's response back to the comparators, is a drawback of certain prior ATE systems that is recognized in the application (page 2, lines 11-

24). The separate test and receive channels used by Iorga et al. suffer from this drawback, which is relieved by applicants' bidirectional passive matching network. The requirement in new claims 11-20 that the passive matching network be "bidirectional" is thus a patentable distinction over the substance of Iorga et al., as is the requirement in new claims 12-14 and 18-20 that the bidirectional passive matching networks specifically comprise T-coil circuits.

Since all of the claims are now believed to be in proper form for allowance, a Notice of Allowance is respectfully requested.

Respectfully submitted,

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